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# METHOD FOR FABRICATING A SEMICONDUCTOR TRANSISTOR DEVICE HAVING ULTRA-SHALLOW SOURCE/DRAIN EXTENSIONS

## Abstract

A method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions is provided. A silicon substrate having thereon a poly gate structure is prepared. The poly gate structure has sidewalls and a top surface. An offset spacer is formed on its sidewall. An ion implantation process is carried out to form an ultra-shallow junction doping region in the silicon substrate next to the offset spacer. An oxide liner is deposited on the offset spacer and on the top surface of the poly gate structure. A tensile nitride spacer layer is then deposited on the oxide liner. A stress modification implantation process is performed to turn the tensile nitride spacer layer into a more compressive status. A dry etching process is then carried out to etch the nitride spacer layer so as to form a spacer.